--FIELD OF THE INVENTION:

The present invention relates to processors and more particularly concerns protocol processors.

BACKGROUND OF THE INVENTION:

The tendency to denser and denser integration of computer hardware leads to the requirement to have greater and greater computational power available for this hardware.--

Page 2, lines 6-11, change:

[The invention therefore aims to create a special processor architecture oriented towards protocol processing and having a very simple structure which is not costly in numbers of transistors, yet makes it possible to unburden the main processor of a system, of simple tasks which are poorly suited to its complexity.]

to instead be:

--SUMMARY OF THE INVENTION:

The invention therefore aims to create a special processor architecture oriented towards protocol processing and having a very simple structure which is not costly in numbers of transistors, yet makes it possible to unburden the main processor of a system, of simple tasks which are poorly suited to its complexity.--

Page 2, lines 23-26, change:

[The invention will be better understood with the aid of the description which will follow, given merely by way of example and made with reference to the attached drawings, in which:]

to instead be:

--BRIEF DESCRIPTION OF THE DRAWINGS:

The invention will be better understood with the aid of the description which will follow, given merely by way of example and made with reference to the attached drawings, in which:--

Page 3, lines 35-38, change: (marked-up version)

[As already indicated in the preamble of the present description, in every application there exist different information processing needs, among which can be distinguished scalar processing and vector processing.]

to instead be:

--DETAILED DESCRIPTION OF THE INVENTION:

As already indicated in the preamble of the present description, in every application there exist different information processing needs, among which can be distinguished scalar processing and vector processing.--

IN THE SPECIFICATION: (clean version)

Page 1, lines 1-6, change:

"The present invention relates to processors and more particularly concerns protocol processors.

The tendency to denser and denser integration of computer hardware leads to the requirement to have greater and greater computational power available for this hardware."

to instead be:

--FIELD OF THE INVENTION:

The present invention relates to processors and more particularly concerns protocol processors.

BACKGROUND OF THE INVENTION:

The tendency to denser and denser integration of computer hardware leads to the requirement to have greater and greater computational power available for this hardware.--

Page 2, lines 6-11, change:

"The invention therefore aims to create a special processor architecture oriented towards protocol processing and having a very simple structure which is not costly in numbers of transistors, yet makes it possible to unburden the main processor of a system, of simple tasks which are poorly suited to its complexity."

to instead be:

--SUMMARY OF THE INVENTION:

The invention therefore aims to create a special processor architecture oriented towards protocol processing and having a very simple structure which is not costly in numbers of transistors, yet makes it possible to unburden the main processor of a system, of simple tasks which are poorly suited to its complexity.--

Page 2, lines 23-26, change:

--The invention will be better understood with the aid of the description which will follow, given merely by way of example and made with reference to the attached drawings, in which:--

to instead be:

--BRIEF DESCRIPTION OF THE DRAWINGS:

The invention will be better understood with the aid of the description which will follow, given merely by way of example and made with reference to the attached drawings, in which:--

Page 3, lines 35-38, change:

"As already indicated in the preamble of the present description, in every application there exist different information processing needs, among which can be distinguished scalar processing and vector processing."

to instead be:

--DETAILED DESCRIPTION OF THE INVENTION:

As already indicated in the preamble of the present description, in every application there exist different information processing needs, among which can be distinguished scalar processing and vector processing.--

IN THE CLAIMS - (marked-up version):

17. (amended) The apparatus of Claim 6, wherein said synchronizing circuit ensures that only one of said first and second processors utilizes said memory circuit for coupling said local memory of said first processor to said local memory of said second processor, at any one time.

19. (amended) The apparatus of Claim 6, wherein an instruction set is provided to said protocol processor, comprising at least one field of execution conditions which is intended therefor and comprises at least the following classes of instructions:

integers corresponding to arithmetic and logic operations on integer numbers;

transfer corresponding to the transfer operations between a register in said first [protocol] processor and memory;

monitoring corresponding to the monitoring of all of the operations modifying the value of an incrementation register in said protocol processor.

IN THE CLAIMS - (clean version):

17. (amended) The apparatus of Claim 6, wherein said synchronizing circuit ensures that only one of said first and second processors utilizes said memory circuit for coupling said local memory of said first processor to said local memory of said second processor, at any one time.

19. (amended) The apparatus of Claim 6, wherein an instruction set is provided to said protocol processor, comprising at least one field of execution conditions which is intended therefor and comprises at least the following classes of instructions:

integers corresponding to arithmetic and logic operations on integer numbers;

transfer corresponding to the transfer operations between a register in said first processor and memory;

monitoring corresponding to the monitoring of all of the operations modifying the value of an incrementation register in said protocol processor.

REMARKS

Applicants have amended the specification to include section headings as requested by the Examiner.

Applicants object to the Examiner's request that Figure 1 include a legend such as --Prior Art--. Nowhere do Applicants state that what is disclosed in Figure 1 is "old" or "prior art". Indeed, Applicants specifically state that: "in low-cost application it is **endeavored** to minimize the number of processors ..." (page 4, lines 1-3). Applicants fail to understand how the above statement can be interpreted to mean "prior art". Accordingly, Figure 1 has not been amended to include the legend "prior art".

Claims 17 and 19 have been amended better to define the claimed invention and overcome the 35 U.S.C. 112, second paragraph, rejections.

Applicants respectfully traverse the Examiner's objection to the term "core" in claims 6 and 36-39, as being given a meaning repugnant to the usual meaning of the term. The Examiner states that the accepted meaning of the term "core" is "one of the types memory built into computers before RAM or main memory." Applicants submit herewith a copy of